ABSTRACT OF THE DISCLOSURE

A nonvolatile semiconductor memory is disclosed, which comprises a nonvolatile memory cell array, a write circuit which repeatedly executes a write and a verification, and a write voltage control circuit, the write voltage control circuit comprising a first binary counter which counts a first clock signal supplied every time the verification fails and supplies output data to the write circuit, a first register which stores data for setting the number of erases and verifications, a second binary counter which is reset using a first timing, counts a second clock signal supplied if a verify write executed on the target write unit fails, an accumulative value storage circuit which is reset using a second timing and stores a value corresponding to an accumulative value for the contents of the second binary counter, and a nonvolatile storage element which stores the appropriate value for the write start voltage.